PATENT ABSTRACTS OF JAPAN

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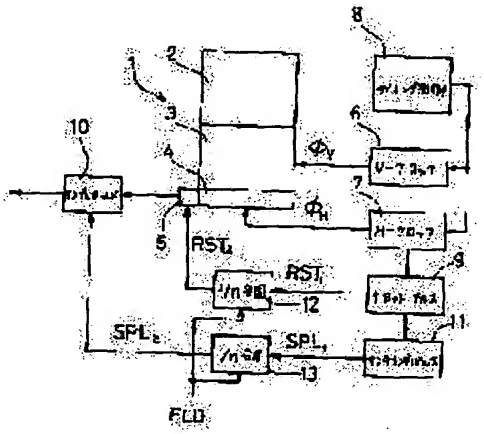
(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:
PURPOSE: To obtain a sufficient output level from an imaging device even if the brightness of an object decreases by mixing plural information charges which occur at each picture element of an imaging device so as to increase the information charge quantity.
CONSTITUTION: The cycle of a reset pulse RST2 which discharges information charges at an output part 5 of an image sensor 1 is set to be n times of the cycle of a horizontal transfer clock ϕH which transfers and drives a horizontal transfer part 4, and the information charges equal to two picture elements are accumulated at output part 5 so as to take out a voltage value. Then the reset timing of timing reset pulse RST2 is set by shifting it by the amount equal to one cycle of the horizontal transfer clock ϕH for each horizontal scanning period and the combination of picture elements which synthesize information charge is shifted by one picture element for each horizontal line at the output part 5. As a result, interlace scanning is also performed in a pseudo manner in the horizontal direction, and so, deterioration of horizontal resolution is prevented.



LEGAL STATUS

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CLAIMS

[Claim(s)]
[Claim 1] While each output of two or more perpendicular transfer sections arranged in parallel mutually is combined with each bit of the level transfer section The solid state image pickup device which outputs the voltage value according to the amount of charges which receives the output of this level transfer section in the output section, and is accumulated at this output section, The information charge of the above-mentioned perpendicular transfer circles is transmitted to the above-mentioned level transfer section for every 1 level line. The driving means which discharge the information charge accumulated at the above-mentioned output section synchronizing with the transfer operation of the above-mentioned level transfer section after transmitting to the above-mentioned output section from the above-mentioned level transfer section furthermore, It has the detection means which takes out the voltage value outputted from the above-mentioned output section synchronizing with discharge operation of the above-mentioned driving means. the above-mentioned driving means The solid state camera characterized by for one period of the transfer operation of the above-mentioned level transfer section period-shifting the timing of discharge operation of the above-mentioned output section, and setting it up for every horizontal scanning period while setting the period of discharge operation of the above-mentioned output section as the integral multiple of the period of the transfer operation of the above-mentioned level transfer section.
[Claim 2] The solid state camera according to claim 1 characterized by delaying for every horizontal scanning period odd-numbered during the vertical scanning, advancing timing of eccrisis operation of the above-mentioned output section for every horizontal scanning period even-numbered during the vertical scanning, and setting it up.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates especially to improvement in light-receiving sensitivity about the solid state camera equipped with CCD series.

[0002]

[Description of the Prior Art] In image pck-up equipments, such as a television camera using CCD series, each scanning timing of image sensors is set up based on the television synchronizing signal according to a predetermined method, and the video signal corresponding to the method of a television synchronizing signal is created. For example, in the case of an NTSC color TV system, the video signal with which a vertical-scanning period is set as 1 / 60 seconds, a horizontal scanning period is further set as 2/525 of vertical-scanning periods, and image information continues per 1 horizontal scanning period is outputted.

[0003] Drawing 6 is the block diagram showing the fundamental composition of the image pck-up equipment which uses CCD series. Frame transfer type CCD series 1 consists of the level transfer section 4 which transmits horizontally the image pck-up section 2 which generates an information charge in response to the image from a photographic subject, the accumulation section 3 which once accumulates an information charge, and an information charge, and outputs it, and the information charge generated in the image pck-up section 2 is transmitted to the accumulation section 3 during [each] the vertical scanning, and it is outputted through the level transfer section 4 for every horizontal scanning period from this accumulation section 3. The output section 5 which changes the amount of information charges into a voltage value is formed in the output side of the level transfer section 4, and the information charge outputted from the level transfer section 4 is accumulated per 1 bit. The perpendicular transfer clock generating circuit 6 and the level transfer clock generating circuit 7 are connected to these image sensors 1, and perpendicular transfer clock phiV of four phases and level transfer clock phiH of two phases are supplied to the accumulation section 3 and the level transfer section 4 of image sensors 1, respectively. The timing-control circuit 8 which sets a vertical-scanning period and a horizontal scanning period to these transfer clock generating circuits 6 and 7 is connected, and the scanning timing of image sensors 1 is matched with a predetermined television system. Moreover, the reset pulse generating circuit 9 which operates synchronizing with the level transfer clock generating circuit 7 is connected to the output section 5 of image sensors 1, and the reset pulse RST which synchronized with level transfer clock phiH is impressed to it. The diffusion field which becomes independent of other fields called floating diffusion electrically is established in this output section 5, and it is constituted so that the information charge accumulated to this diffusion field may be discharged by the drain for charge discharge according to a reset pulse RST. That is, a reset pulse RST is set up so that the information charge may be discharged, whenever the information charge of the level transfer section 4 is transmitted to the output section 5, since the output section 5 accumulated the information charge transmitted to the output section 5 from the level transfer section 4 to the diffusion field in the output section 5 and the voltage value has been acquired from change of the potential of a diffusion field. Therefore, the output to which potential is changed to the timing according to the reset pulse RST is obtained from the output section 5, and this output is incorporated by the sample hold circuit 10. Like the reset pulse generating circuit 9, the sampling-pulse generating circuit 11 which supplies a sampling pulse SPL to a sample hold circuit 10 synchronizes with the level transfer clock generating circuit 7, and sets sampling timing as timing slightly earlier than the reset timing of a reset pulse RST. Only the voltage value corresponding to the amount of information charges outputted from the level transfer section 4 among the output voltage of the output section 5 is taken out by this, and it is outputted to the circuit of the next step as a video signal.

[0004] In the above image pck-up equipments, although the period which accumulates the information charge for one screen in the image pck-up section 2 is set up as for example, 1 / 60 seconds, it is also possible by discharging the information charge of the image pck-up section 2 to specific timing to set an accumulation period as 1 / 60 seconds or

less. Therefore, to a bright photographic subject, the accumulation period of an information charge was set up short and the saturation of the image pck-up section 2 of image sensors 1 is prevented. On the contrary, it is continuing and setting the accumulation period of an information charge as two or more vertical-scanning periods to a dark photographic subject, an accumulation period is made into 1 / 60 seconds or more, and it is constituted so that a part for a underexposure may be compensated. In this case, since a transfer of the information charge from the image pck-up section 2 to the accumulation section 3 is performed every 1 vertical-scanning period, the output of image sensors 1 will be obtained every 1 vertical-scanning period. Therefore, to the output of image sensors 1, processing which interpolates a signal per vertical-scanning period is performed. Image pck-up equipment equipped with such an exposure control function is proposed by for example, these people at Japanese Patent Application No. No. 66330 [63 to].

[0005]

[Problem(s) to be Solved by the Invention] However, in interpolating to the output of image sensors 1, the field memory which memorizes the signal for one screen is needed, and it has the problem that a circuit scale becomes large. Then, it considers increasing the amount of information charges and improving the sensitivity on the appearance of image sensors 1 by compounding the information charge for 2 pixels of the image pck-up section 2. In case the information charge for 2 pixels is compounded, the method of compounding in the transfer process of an information charge and the method of compounding at the time of conversion to the voltage value in the output section 5 are used. When compounding an information charge in transfer process, 2 pixels of a perpendicular direction will be compounded by operating the level transfer section 4 every 1 horizontal scanning period. In this case, since the output of image sensors 1 is obtained every 1 horizontal scanning period, it will be necessary to interpolate the output of image sensors 1 per horizontal scanning period. On the other hand, by setting discharge operation of the charge of the output section 5 as the period of the double precision of the transfer operation of the level transfer section 4, when compounding an information charge in the output section 5, it is constituted so that the information charge for 2 pixels may be accumulated in the output section 5 and it may change into a voltage value.

[0006] Although it sees by the rise of the output level from image sensors 1 and the upper sensitivity improves in compounding the information charge of two or more pixels as mentioned above and obtaining a video signal, resolution falls for reduction of the amount of information by mixture of two or more pixels. Especially about horizontal resolution, it becomes the obstacle of the improvement in quality of image of eye a difficult hatchet and a reproduction screen to compensate the fall of resolution by the conventional interlace drive.

[0007] Then, this invention aims at offer of the solid state camera which can aim at improvement in sensitivity, preventing the fall of resolution.

[0008]

[Means for Solving the Problem] The place by which accomplished in order that this invention might solve an above-mentioned technical problem, and it is characterized [the] While each output of two or more perpendicular transfer sections arranged in parallel mutually is combined with each bit of the level transfer section The solid state image pickup device which outputs the voltage value according to the amount of charges which receives the output of this level transfer section in the output section, and is accumulated at this output section, The information charge of the above-mentioned perpendicular transfer circles is transmitted to the above-mentioned level transfer section for every 1 level line. The driving means which discharge the information charge accumulated at the above-mentioned output section synchronizing with the transfer operation of the above-mentioned level transfer section after transmitting to the above-mentioned output section from the above-mentioned level transfer section furthermore, It has the detection means which takes out the voltage value outputted from the above-mentioned output section synchronizing with discharge operation of the above-mentioned driving means. the above-mentioned driving means While setting the period of discharge operation of the above-mentioned output section as the integral multiple of the period of the transfer operation of the above-mentioned level transfer section, it is in one period of the transfer operation of the above-mentioned level transfer section period-shifting the timing of discharge operation of the above-mentioned output section, and setting it up for every horizontal scanning period.

[0009]

[Function] According to this invention, by one period of the transfer operation of the above-mentioned level transfer section period-shifting the timing of discharge operation of the above-mentioned output section, and setting it up for every horizontal scanning period, the combination of the pixel of the information charge compounded in the output section shifts by 1 pixel with each level line, and 1 pixel of video signals obtained from an element shifts for every level line. Therefore, if the video signal is reproduced, it will be indicated by the interlace horizontally in false.

[0010]

[Example] Drawing 1 is the block diagram showing one example of this invention solid state camera. In this drawing,

image sensors 1 and its drive circuit (the perpendicular transfer clock generating circuit 6 and level transfer clock generating circuit 7) are the same as that of drawing 6 , and they are constituted so that perpendicular transfer clock phiV and level transfer clock phiH may be supplied to image sensors 1 and may be driven according to the scanning timing set up by the timing-control circuit 8.

[0011] The place by which it is characterized [of this invention] is by impressing the reset pulse RST2 which has one n times (n is an integer) the period of level transfer clock phiH to the output section 5 of image sensors 1 to accumulate the information charge outputted from the level transfer section 4 in the output section 5 every n pixels, and change into a voltage value. Drawing 2 is the timing chart showing operation in the case of compounding the information charge for 3 pixels in the output section 5 by setting up the period of a reset pulse RST2 by 3 times the level transfer clock phiH.

[0012] After the reset pulse RST1 which has the same period as level transfer clock phiH is outputted from the reset pulse generating circuit 9 and 1 / 3 dividing are carried out by the frequency divider 12, it is supplied to the output section 5 as a reset pulse RST2 which has one 3 times the period of level transfer clock phiH. For this reason, discharge operation of the output section 5 turns into transfer operation 3 times the period of the level transfer section 4, and the information charge horizontal to the output section 5 for 3 pixels is accumulated.

[0013] By the way, dividing operation of the reset pulse RST2 in a frequency divider 12 answers the field distinction signal reversed for every (every vertical-scanning period) field, is performed to the timing which is overdue by one period of level transfer clock phiH for every horizontal scanning period in the odd number field ODD, and is performed to the timing which progresses by one period of level transfer clock phiH for every horizontal scanning period in the even number field EVEN. Therefore, the reset pulse RST2 supplied to the output section has the phase in which a position of the 3rdn horizontal scanning period and the horizontal scanning period of eye ** (3n+1) watch differ from the horizontal scanning period of eye ** (3n+2) watch, respectively, as shown in drawing 2 . For example, in the case of the odd number field ODD, in a position of the 3rdn horizontal scanning period, a frequency divider 12 is reset in the standup of the horizontal scanning signal HD. In level transfer clock phiH of eye ** (3n+1) watch, it is late from the standup of the horizontal scanning signal HD by one period of level transfer clock phiH, and a frequency divider 12 is reset. And it constitutes from a horizontal scanning period of eye ** (3n+2) watch so that it may be late from the standup of the horizontal scanning signal HD by two periods of level transfer clock phiH and a frequency divider 12 may be reset. According to such a reset pulse RST2, 1 pixel of combination of the pixel by which discharge operation of the information charge of the output section 5 is compounded in the output section 5 since only one period of level transfer clock phiH shifts for every horizontal scanning period to the transfer operation of the level transfer section 4 will shift for every level line.

[0014] Although incorporated by the sample hold circuit 10, the output from this output section 5 is set up about the timing of this sampling action so that it may correspond to eccrisis operation of the output section 5. Therefore, dividing of the sampling pulse SLP 1 outputted from the sampling-pulse generating circuit 11 is carried out to one third by the frequency divider 13, and it is supplied to a sample hold circuit 10 as a sampling clock SLP 2 which has one 3 times the period of level transfer clock phiH. Moreover, about the timing of a sampling, as well as the case of drawing 6 since it is necessary to make it early smaller than the eccrisis timing of the information charge of the output section 5, a sampling clock SLP 1 is set as the phase which progressed slightly to the reset pulse RST1.

[0015] And it is expressed by the same data every 3 pixels which the pixel O of odd lines surrounds with a dashed line with combination with interlace scanning in the odd number field as shown in drawing 3 , and is expressed by the same data in the even number field every 3 pixels which the pixel E of even lines surrounds with a dashed line. Therefore, since interlace scanning is carried out also horizontally in false at the same time interlace scanning is carried out perpendicularly, in spite of compounding the 3-pixel information charge horizontally, the fall of horizontal resolution is oppressed.

[0016] Drawing 4 is drawing showing the synthetic state of an information charge in case a 2-pixel information charge is compounded, and drawing 5 is the timing of operation in that case. In this case, for every horizontal scanning period, only one period of level transfer clock phiH shifts, and dividing operation of the reset pulse RST1 in a frequency divider 12 is set up. That is, by resetting a frequency divider 12 in the standup of the horizontal scanning signal HD, being late from the standup of the horizontal scanning signal HD by one period of level transfer clock phiH even-numbered during the horizontal scanning, and resetting a frequency divider 12, during the whole horizontal scanning, mutually, it shifts by one period of a reset pulse RST1, and the reset timing of a reset pulse RST2 is set to the odd-numbered horizontal scanning period, as shown in drawing 5 . At this time, dividing operation of a frequency divider 13 is set up so that sampling timing may shift by one period of level transfer clock phiH for every horizontal scanning period about the sampling pulse SLP 2 as well as a reset pulse RST2. Thus, since the reset pulse RST2 of SOREZORE is in agreement by the case where a reset pulse RST2 is delayed a term 1 round of level transfer clock phiH, and the

case where it advances conversely in compounding a 2-pixel information charge, the reset pulse RST2 of the odd number field ODD and the even number field EVEN becomes the same.

[0017] In the above example, although the case where 3 or a 2-pixel information charge was compounded was illustrated, it is also possible to compound an information charge 4 pixels or more. In this case, although it becomes a quite coarse reproduction screen, according to the image pck-up element of the high resolution into which the pixel pitch turned minutely, the granularity of a reproduction screen stops being able to be conspicuous easily.

[0018]

[Effect of the Invention] According to this invention, while making sensitivity of image pck-up equipment high, by oppressing the fall of the resolution accompanying the improvement in sensitivity, it is high sensitivity and the high image pck-up equipment of resolution can be realized. Moreover, since the thing of the structure as the conventional thing with the same image pck-up element itself is employable, improvement in sensitivity can prevent elevation of eye a possible hatchet and cost easily by change of the scanning timing of a drive circuit.

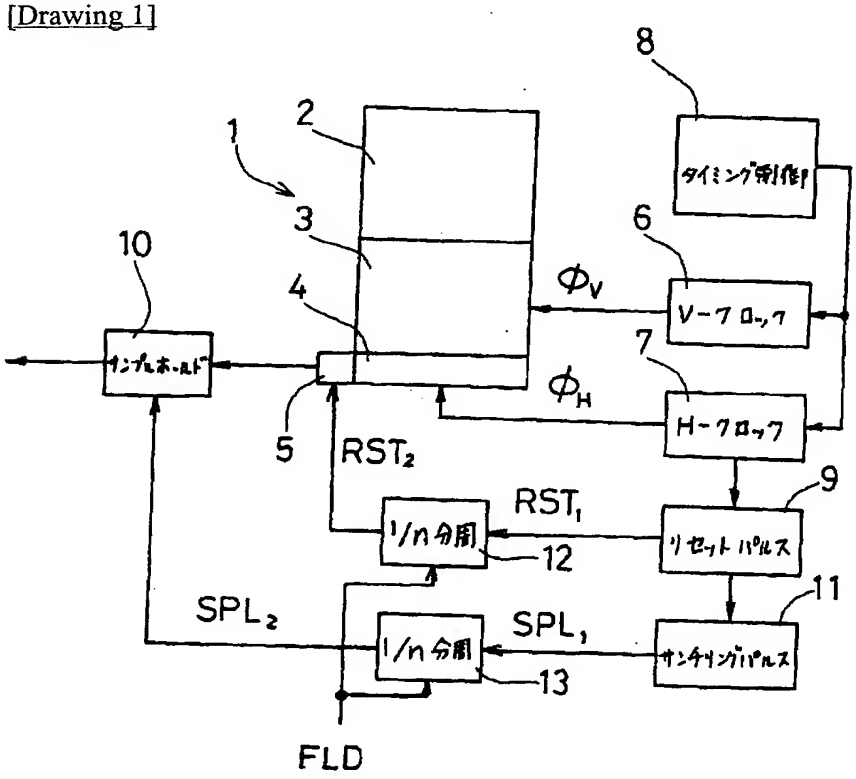
[Translation done.]

* NOTICES *

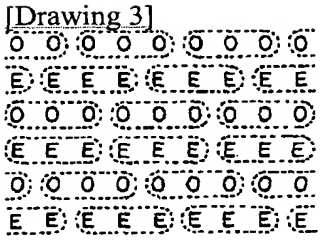
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

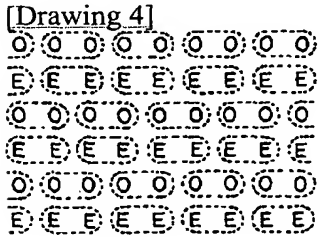
[Drawing 1]



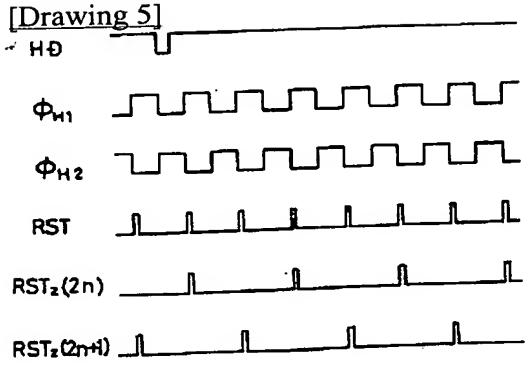
[Drawing 3]



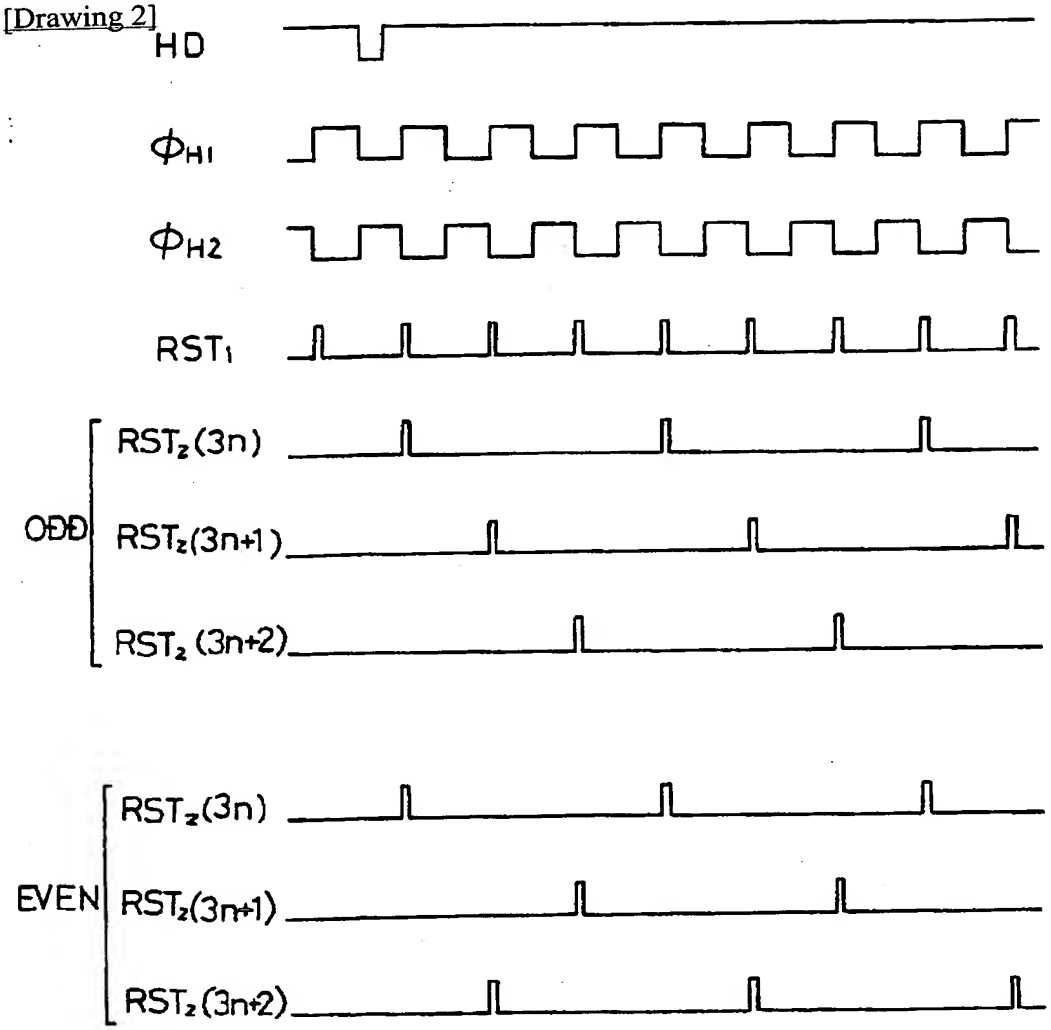
[Drawing 4]



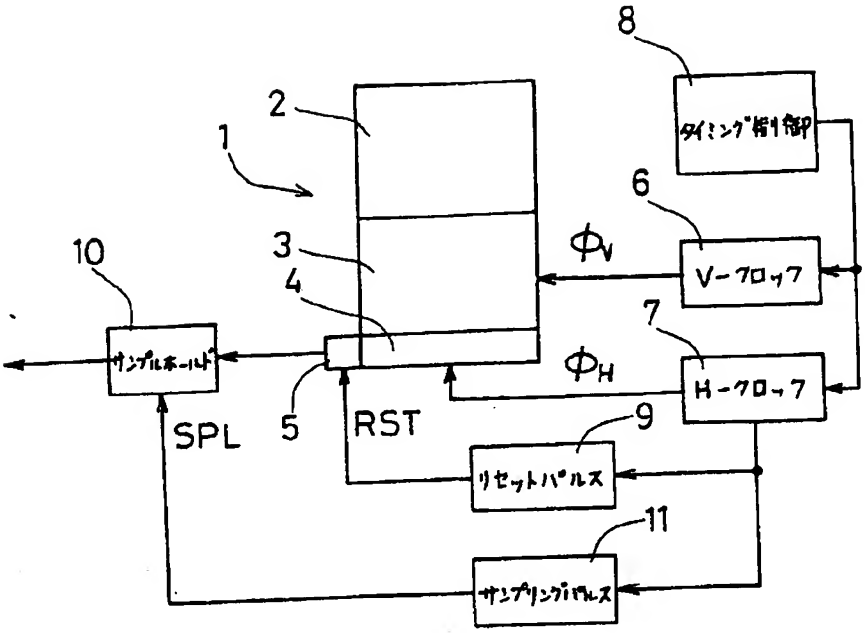
[Drawing 5]



[Drawing 2]



[Drawing 6]



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